WHAT IS CLAIMED IS:

1. A semiconductor element comprising:

a substrate;

a first DMOS element formed on a first portion of the substrate, wherein the DMOS element includes a gate electrode having slanted side walls; and

a first MOS element formed on a second portion of the substrate that is separate from the first portion.

2. The semiconductor element of claim 1, wherein the slanted side walls of the gate electrode of the first DMOS element and side walls of a gate electrode of the first MOS element have different profiles.

3. The semiconductor element of claim 1, wherein the first DMOS element includes:

a well of a first conductive type formed on the substrate;

a body region of a second conductive type formed in the well;

a source region of the first conductive type formed in the body region;

a drain region of the first conductive type formed in the well and spaced from the source region; and

a gate insulating layer formed between the well and the gate electrode.

4. The semiconductor element of claim 3, wherein a part of the source region overlaps a portion of one of the slanted side walls.

5. The semiconductor element of claim 1, wherein the first MOS element includes:

a well of a first conductive type formed on the substrate;

a source region of a second conductive type formed in the well;

a drain region of the second conductive type formed in the well;

a gate electrode formed on the well of the first conductive type; and

a gate insulating layer interposed between the gate electrode and the well of the first conductive type.

6. The semiconductor element of claim 1, wherein a gate insulating layer of the first DMOS element includes a relatively thicker portion.

7. The semiconductor element of claim 5, further comprising:

a protection layer covering the first MOS element and the first DMOS element, wherein the protection layer has first and second contact holes that expose a source region of the first DMOS element and a drain region of the first DMOS element, and wherein the protection layer has third and fourth contact holes formed in the protection layer to expose the source region of the first MOS element and the drain region of the first MOS element;

a source electrode that contacts the source region of the first DMOS element through one of the first and second contract holes;

a drain electrode that contacts the drain region of the first DMOS element through the other one of the first and second contact holes;

a source electrode that contacts the source region of the first MOS element through one of the third and fourth contact holes; and

a drain electrode that contacts the drain region of the first MOS element through the other one of the third and fourth contact holes.

8. The semiconductor element of claim 1, further comprising:

a second DMOS element formed on the substrate opposing the first DMOS element; and

a second MOS element formed on the substrate opposing the first MOS element.

9. The semiconductor element of claim 8, wherein the second DMOS element includes a gate electrode having slanted side walls.

10. A semiconductor element comprising:

a substrate;

a DMOS element formed in a first region of the substrate, wherein the DMOS element includes a gate electrode having slanted side walls;

a CMOS element formed in a second region of the substrate; and

a bipolar element formed in a third region of the substrate.

11. A method for manufacturing a semiconductor element, comprising

preparing a substrate that defines a first DMOS element region and a first MOS element region;

forming a first gate electrode on the substrate in the DMOS element region, wherein the first gate electrode includes slanted side walls; and

forming a second gate electrode on the substrate in the MOS element region.

12. The method of claim 11, wherein the second gate electrode element is formed to have a side wall profile different from the slanted side walls of the gate electrode of the DMOS element.

13. The method of claim 11, wherein preparing the substrate comprises:

forming a first buried layer in the DMOS element region;

forming a second buried layer in the MOS element region;

forming an epitaxial layer over a surface of the substrate;

forming a first conductive well in the epitaxial layer in the DMOS element region;

forming a second conductive well in the epitaxial layer in the MOS element region; and

forming a field oxidation layer between the first conductive well and the second conductive well so that the field oxidation layer separates the DMOS element region and the MOS element region.

14. The method of claim 13, comprising forming the field oxidation layer using a LOCOS process.

15. The method of claim 13, further comprising forming a sectional oxidation layer on a portion of the first well.

16. The method of claim 13, further comprising:

forming a conductive body region in the first well following the formation of the first gate electrode; and

forming a source region in the first well after the second gate electrode is formed;

forming a drain region in the first well after the second gate electrode is formed;

forming a source region in the second well after the second gate electrode is formed; and

forming a drain region in the second well after the second gate electrode is formed.

17. The method of claim 11, further comprising injecting channel ions into the MOS element after the first gate electrode is formed.